

REMARKS

Reconsideration of the application is respectfully requested in view of the following remarks. Claims 1-31 were pending in the application prior to this amendment. Claims 32-43 have been added to the application with this amendment. Claims 7-15 and 22-30 have been allowed.

The May 9, 2003 Office Action objected to claims 2, 3, 5, 17, 18, and 20. These claims have been amended to convert the claims to independent form and to place the claims in condition for allowance.

Rejection under 35 USC 102(b)

In the Office Action, claims 1, 4, 6, 16, 19, 21, and 31 were rejected under 35 U.S.C. 102(b) as being unpatentable over Giomi et al. (Giomi), U.S. Patent No. 5,537,580. For a 102(b) rejection to be proper, the cited art must show each and every element as set forth in a claim. (See MPEP § 2131). However, Giomi does not disclose each and every element. Accordingly, the rejection is respectfully traversed and should now be withdrawn. The remarks below are based on the present understanding of Giomi.

In Giomi (as currently understood) an integrated circuit behavior description, provided in HDL, is converted into a register-transfer level intermediate description. (Giomi; col. 4, lines 37-45). The intermediate description is represented by a control flow graph. (Giomi; col. 5, lines 18-20). A register-level state transition table is then created, by extracting a state transition table from directed acyclic graphs. (Giomi, col. 7, lines 499-52) A logic-level state transition table is then generated, which is, in turn, used to generate a state machine structural netlist. (Giomi, col. 4, lines 49-51). The structural netlist is then combined with an independently

synthesized structural netlist to create an integrated circuit (IC) structural netlist. (Giomi, col. 3, lines 43-46). The IC netlist is then used in chip compilation (Giomi, Fig. 1b, blocks 19-20.)

Claim 1 now requires the act of “condensing the expanded conversion matrix to a condensed generic format.” Support for this requirement is found in Applicant’s specification at page 24, lines 13-17. Giomi does not have, suggest or disclose “condensing the expanded conversion matrix to a condensed generic format.” In Giomi, after random logic netlists (Giomi, Fig. 1b, block 19) and logic level state machine description netlists are generated (Fig. 1b, block 18), they are combined, (Giomi, Fig. 1b, at block 19) and then used “to provide a basis for chip compilation....” (Giomi, Abstract and Fig. 1b, at block 20.) No condensation of an expanded conversion matrix is disclosed. Moreover, there is no motivation to do so, as the IC netlist itself is used by the chip compilation step.

Also, Giomo nowhere discloses “determining a generic HDL register and a plurality of generic HDL input logic for the generic HDL register to replicate the behavior represented by the data structure based on the condensed conversion matrix” (emphasis added).

Thus, for at least the reasons discussed above, Applicants respectfully submit that claim 1 is not anticipated by Giomi, and should be allowed.

New claims 32 and 36 depend directly from claim 1, and are allowable for the reasons given above in support of their parent claim. In addition, these claims each are independently patentable. For example, claim 32 is separately patentable by reason of the method act “whereby the condensing further comprises using a Karnaugh map.” As another example, claim 36 is separately patentable by reason of the method act “wherein determining provides identical HDL registers for data structures with different representations but identical functionality.”

Claim 4 has been written in independent format and, we respectfully suggest, is allowable in its present form. This amendment has not been made to overcome a statutory rejection and therefore does not limit the equivalence of any claim element under the Doctrine of Equivalents.

Claim 4 is patentable by reason of the method act “wherein the conversion matrix comprises a plurality of entries representing every state of the circuit element and every corresponding next state of the circuit element.” (emphasis added). Giomi is not understood to disclose a method comprising “representing every corresponding next state of the circuit element.” Rather, Giomi, as cited here, speaks of deliberately using less than every state--“In order to reduce the complexity of state value extraction, the extraction method of the preferred embodiment partially derives values from the leave data-element nets and does not extract all implicit state values for a given acyclic graph.” (See Giomi, col. 8, at lines 58-62.) This is reinforced by an upper limit imposed on the possible number of state values allowed to be extracted. In Giomi, a counter is incremented after each state value is extracted. (Fig. 4, step 66.) If the counter exceeds a Max State Value, Fig 4, step 67, then an error occurs. (Giomi, Fig. 4, unnumbered node.) Because only a limited number of state values can be extracted before there is an error, Giomi teaches away from extracting all state values. It is submitted that nowhere does Giomo teach or suggest “a plurality of entries representing every state of the element” let alone in the combination of claim 4. Applicant, therefore, respectfully suggests that claim 4 is in condition for allowance.

Claim 6 has been rewritten in independent form. This amendment has not been made to overcome a statutory rejection and therefore does not limit the equivalence of any claim element under the Doctrine of Equivalents.

Applicants respectfully suggest that claim 6 is allowable in its current form. Claim 6 is patentable by reason, at least, of the method act of “populating entries of the conversion matrix for each state transition.” (Emphasis added.) Giomi specifically states that not all state transitions have entries in the conversion matrix. “The state transition table is build incrementally at each evaluation. With this method, only a subset of implicit state values are found. This subset is sufficient to extract most or all behavioral state machine descriptions.” Giomi, col. 9, lines 33-37. If some state values are missing, then their transitions will also be absent. The examiner is asked to point to any disclosure in Giomi of a conversion matrix that is populated with entries for each state transition, let alone in the combination in claim 6. Applicant, therefore, respectfully suggests that claim 6 is in condition for allowance.

Independent claim 16 has been amended to require “determining a generic HDL register and a plurality of generic HDL input logic comprising combinational gates for the generic HDL register to replicate the behavior represented by the data structure based on the conversion matrix.” Support for the change can be found in the applicants’ specification at page 10, lines 1-13. Giomi neither suggests nor discloses the requirements in claim 16. Giomi, rather, extracts state machines from a functional description of an integrated circuit (Giomi, col. 3, lines 48-52), and then processes these state machines to generate netlists. (Giomi, Fig. 1b at 15-19). The netlists are then used in IC Chip compilation. (Giomi, Fig. 1b, at 20). The netlists are not further modified before they are used in IC chip compilation. (Giomi, Fig. 1b.) Further, there is no motivation to modify the netlists between the time they are combined and their use in IC compilation as the netlists are created “to provide a basis for chip compliation...” (Giomi, Abstract.)

Nowhere is Giomi understood to disclose a “generic HDL register and a plurality of generic HDL input logic comprising combinatorial gates” being produced which “replicate the behavior represented by the data structure based on the conversion matrix” as is required in claim 16. The examiner is asked to point to any disclosure in Giomi of an HDL register being determined by a conversion matrix let alone all the requirements of “a generic HDL register and a plurality of generic HDL input logic comprising combinatorial gates” being determined by a conversion matrix. Applicants respectfully suggest, therefore, that claim 16 is in condition for allowance.

Claim 21 and new claims 33-35, 42, and 43 depend directly or indirectly from claim 16, and are allowable for the reasons given above in support of their parent claim. Moreover, each of these claims are independently patentable. For example, claim 21 is separately patentable by reason, at least, of the processor executing machine readable instructions of “populating entries of the conversion matrix for each state transition.” As another example, claim 33 is separately patentable by reason, at least, of the processor executing machine readable instructions of “classifying a conversion matrix column into a category, the category comprising an edge state, a level state, a reachable state, or an unreachable state.” As yet another example, claim 34 is separately patentable by reason at least of “classifying a column as an output state transition.” As a further example, claim 35 is separately patentable by reason, at least, of the processor executing machine readable instructions of the output state transition comprising “one of $QQ+=00$, $QQ+=01$; $QQ+=0X$, $QQ+=10$, $QQ+=11$; or $QQ+=1X$.”

As yet another example, claim 42 is separately patentable by reason, at least, of the processor executing machine readable instructions “wherein the conversion matrix comprises a plurality of entries representing every state of the circuit element.” As a final example, claim 43

is separately patentable by reason, at least, of the processor executing machine readable instructions “wherein the plurality of entries representing every state of the circuit further comprise every next reachable state of the circuit element.”

Claim 19 has been written in independent form. This amendment has not been made to overcome a statutory rejection and therefore does not limit the equivalence of any claim element under the Doctrine of Equivalents.

The current claim 19 is patentable by reason, at least, of the processor executing machine readable instructions “wherein the conversion matrix comprises a plurality of entries representing every state of the circuit element and every corresponding next state of the circuit element.” Giomi is not understood to disclose a method comprising “every state of the circuit element.” Rather, language in Giomi (as presently understood) speaks of deliberately using less than every state: “In order to reduce the complexity of state value extraction, the extraction method of the preferred embodiment partially derives values from the leave data-element nets and does not extract all implicit state values for a given acyclic graph.” (Giomi, col. 8, lines 58-62.) This is reinforced by an upper limit imposed on the possible number of state values allowed to be extracted. In Giomi, a counter is incremented after each state value is extracted. (Fig. 4, step 66.) If the counter exceeds a Max State Value, (Giomi, Fig 4, step 67) then an error occurs. (Giomi, Fig. 4, unnumbered node.) Because only a limited number of state values can be extracted before there is an error, Giomi strongly suggests that not all state values should be extracted. Therefore, Giomi both explicitly and implicitly limits the number of state values extracted. Giomi also does not teach the conversion matrix comprising “every corresponding next state of the circuit element.” If every state value is not present, then it logically follows that the missing states will correspond to missing next states as well. It is submitted that nowhere

does Giomo teach or suggest “a plurality of entries representing every state of the circuit element” let alone in the combination given in claim 19. Therefore, Applicants respectfully suggest that claim 19 is in condition for allowance.

Independent claim 31 is patentable by reason, at least, of the added apparatus features of “said conversion matrix to represent the data structure in a first compressed format; convert the conversion matrix into a second condensed format, said condensed conversion matrix to represent the behavior of the circuit element in a generic format...” Nowhere is Giomi understood to describe a processor executing machine readable instructions to represent the data structure in a first and a second separate compressed format, let alone in the combination required by claim 31. Therefore, Applicants respectfully suggest that claim 31 is in condition for allowance.

Claim 41 depends directly from claim 31, and is allowable for the reasons given above in support of its parent claim. Moreover, claim 41 is independently patentable by reason, at least, of the requirements “wherein data structures with different representation but identical functionality in the first compressed format are given identical representations in the second compressed format.”

Similarly, new claims 37-40 depend from claim 8 which has been allowed, and so should be in condition for allowance. These claims are also independently patentable. For example claim 37 is independently patentable by reason of the method act “wherein each next state is classified as level (L) or edge (E) sensitive.” As another example, claim 38 is independently patentable by reason of the method act where “each next state is classified as reachable (R) or unreachable (U).” Claim 39 is separately patentable by reason of the the method act “wherein each next state is classified using at least six of the following state transitions (QQ+ =00, 01, 0X,

10, 11, 1X, X0, X1, XX)." As a final example, claim 40 is independently patentable for the method act "wherein each next state is classified without using at least one of the following output state transitions (QQ+ = X0, X1, XX)." .

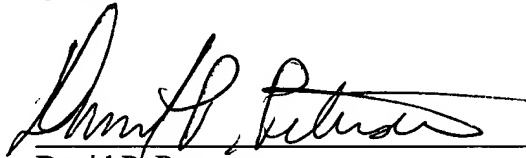
In conclusion, Applicants respectfully submit that claims 1-43 are now in a condition for allowance, and Applicants respectfully request allowance of such claims.

Conclusion

The Applicants respectfully submit that, in light of the arguments herein, all claims are in condition for allowance. An early notice to that effect is respectfully requested. Should any matters remain, the Examiner is respectfully requested to telephone the undersigned, in accordance with MPEP 713.01.

Respectfully submitted,

KLARQUIST SPARKMAN, LLP

By 

David P. Petersen

Registration No. 28,106

One World Trade Center, Suite 1600
121 S.W. Salmon Street
Portland, Oregon 97204
Telephone: (503) 226-7391
Facsimile: (503) 228-9446